Amendments to the Specification:

Please replace the paragraph beginning at page 1, line 2, with the following rewritten paragraph:

This application claims the benefit of U.S. Provisional Application No. 60/190,803 filed March 21, 2000, and is related to commonly owned U.S. Patent Application No. _____ (Attorney Docket APP 1253_1) and to commonly owned U.S. Patent Application No. _____ (Attorney Docket APP 1253_2).

Please replace the paragraph beginning at page 6, line 8, with the following rewritten paragraph:

Each SIC-ATRF processor 204 includes a conventional detector 206, a respread processor 208, an adaptive temporal reconstruction filter (ATRF) 210, and a complex mathematical processor 212. The conventional detector ~~210~~ 206 is connected to the respread processor 208 and the mathematical operations processor 212 of the SIC-ATRF processor in the previous stage. For the SIC-ATRF processor 204 in the first stage, the conventional detector 210 is connected to an external entity providing a processed version of the received signal r(t) and to the respread processor 208. The respread processor 208 is in turn connected to the ATRF 210, which is connected to the mathematical operations processor 212. The output of the mathematical operations processor 212 is connected to the conventional detector 208 of the SIC-ATRF processor of the next stage and the mathematical operations processor 212 of the next stage. For the SIC-ATRF processor 204 in the first stage, the mathematical operations processor 212 is connected to the external entity providing a processed version of the received signal r(t) instead of the mathematical operations processor 212 of a previous stage.

Please replace the paragraph beginning at page 8, line 28, with the following rewritten paragraph:

In step 630, the symbol estimate generated by the conventional detector 206 is mixed with the user codes in the respread processor 208 to generate a scaled estimate of the transmitted signal for the user. Using the scaled estimate as input, the ATRF 210 estimates the channel for the user, (i.e., the multipath components and their associated amplitudes and phases) and reconstructs the signal interference associated with the user signal (step 640). The reconstructed signal for the user is then cancelled from the total received signal r(t) in the mathematical operations processor 212 (step 650). The output of the mathematical operations processor 212 is then input to the SIC-ATRF processor ~~203~~ 204 in the next stage of SIC-MCCE system 200. The output is also fed back to the MCCE weight update processor 64. Steps 620 through 650 are successively repeated for each of the k stages.

Please replace the paragraph beginning at page 12, line 10, with the following rewritten paragraph:

The PIC-MCCE system 900 includes a plurality of parallel processors 905. The number of processors can vary but is typically determined by the number of users associated with the system. Each processor is comprised of a conventional detector 206, a respread processor 208 and an ATRF 910. The conventional detector 206 in each parallel processor 905 is connected to a respread processor 208 and to a single external entity that communicates

the received signal r(t) as input to the conventional detector. The ATRF 910 in each parallel processor 905 is connected between a respread processor 208 and a series 913 of mathematical operations processors 212. Alternatively, a partial summer circuit could be substituted for the series of mathematical operations processors. The series of mathematical operations processors 913 (or alternatively the partial summer circuit) is connected to the ATRF ~~210~~ 910 in every parallel processor 905 and to the external entity providing the received signal.

Please replace the paragraph beginning at page 12, line 22, with the following rewritten paragraph:

The conventional detector 206 and the respread processor 208 are identical to the conventional detector 206 and respread processor 208 used in the SIC-MCCE embodiment. In addition, a control processor ~~902~~ could optionally be included to provide ordering of the signals prior to processing by the PIC-MCCE system.

Please replace the paragraph beginning at page 13, line 18, with the following rewritten paragraph:

A partial PIC-JMCCE system is shown in Figure 11A according to an illustrative embodiment of our invention. In this embodiment, each processor 905 of the PIC-JMCCE system has an individual ATRF 911. In a system with k users, each ATRF 911 receives k input signals, one from each of the respread processors 208 in the other parallel processors 905. Each ATRF 911 processes the signals as described above for step ~~544~~ 640 of SIC-JMCCE processing.

Please replace the paragraph beginning at page 16, line 26, with the following rewritten paragraph:

Figure 13 depicts a single stage of a system 1300 combining STAP, interference cancellation MUD, and minimum cost channel estimation (MCCE) according to a specific illustrative embodiment of our invention. The illustrative embodiment of our invention shown in Figure 13 applies SIC (e.g., SIC-MCCE or SIC-JMCCE) to each antenna element separately. We shall refer to this system as the STAP/VSIC system where the V refers to the vector nature of the cancellation process. The multi-stage STAP/VSIC receivers resemble the multi-stage SIC receivers of ~~figure~~ Figures 2, 4, and 5, except that the received signal and cleaned received signals are now vectors of size M.

Please replace the paragraph beginning at page 17, line 30, with the following rewritten paragraph:

The illustrative system of Figure 14 comprises a plurality of J-STAPSIC processors arranged in successive stages 1404. The input to the J-STAPSIC system 1400 is a vector of size M where M is equivalent to one received signal stream for each antenna ~~element)~~ element. Each stage utilizes the symbols of all previously detected users, and detects one additional user's symbols. The number of stages, K, is equivalent to the total number of users associated with the system.

Please replace the paragraph beginning at page 18, line 2, with the following rewritten paragraph:

An illustrative embodiment of a k^{th} J-STAPSIC stage 1404 is shown in Figure 15. Each J-STAPSIC stage comprises a plurality of STAP filters ~~1252~~ 1250, one per antenna, in a parallel arrangement, a plurality of respread processors, one per previous stage, in a parallel arrangement for receiving the symbol estimates from the previous J-STAPSIC stages, a plurality of ATRF filters 1410, one per previous stage, a mathematical summation circuit 1414 for summing the outputs of the plurality of STAP filters, a mathematical summation circuit 1414 for summing the outputs of the plurality of ATRF filters, a mathematical operations processor 212 for adding the outputs of the mathematical summation circuits 1414, a conventional detector 206, and a respread processor 208.

Please replace the paragraph beginning at page 18, line 11, with the following rewritten paragraph:

In the k^{th} stage, the plurality of STAP filters ~~1252~~ 1250 receive a cleaned vector received signal, $r_1(t)$, $r_2(t)$, ... $r_M(t)$ from the previous stage and the plurality of parallel respread processors receive a vector comprising symbol estimates determined in the previous stage. In each parallel respread processor, the symbol estimates are spread. The mathematical summation circuit 1414 sums the outputs from the plurality of the STAP filters and another mathematical summation circuit sums the outputs from the plurality of ATRF filters. The outputs of these summation circuits are then combined in a mathematical operations circuit 212. Using the output of the mathematical operations circuit 212, the conventional detector despreads the input and estimates the symbol transmitted. The symbol estimate is then spread by the respread processor. The output of the respread processor is combined with the output of the conventional detector and is used as input to an MCCE weight update processor. The MCCE weight update processor then updates in parallel the tap weights of the plurality of STAP and ATRF filters.